N-Channel Power MOSFET

600V, 2A, 4.4Ω

FEATURES

- Advanced planar process
- 100% avalanche tested
- Pb-free plating
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

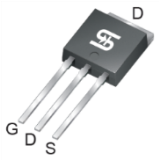
APPLICATION

- Power Supply
- Lighting

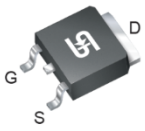
KEY PERFORMANCE PARAMETERS		
PARAMETER	**VALUE**	**UNIT**
V_{DS}	600	V
$R_{DS(on)}$ (max)	4.4	Ω
Q_g	9.4	nC

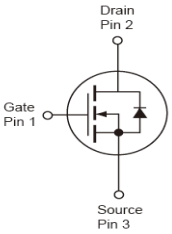
Pb-Free RoHS COMPLIANT HALOGEN FREE

TO-251(IPAK)



TO-252(DPAK)





Notes: MSL 3 (Moisture Sensitivity Level) for TO-252 (D-PAK) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	2	A
	T_C = 100°C		1.35	
Pulsed Drain Current (Note 2)		I_{DM}	8	A
Single Pulsed Avalanche Energy (Note 3)		E_{AS}	55	mJ
Single Pulsed Avalanche Current (Note 3)		I_{AS}	2	A
Repetitive Avalanche Energy (Note 2)		E_{AR}	4.4	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4.5	V/ns
Total Power Dissipation @ T_C = 25°C		P_{DTOT}	44	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\Theta JC}$	2.87	°C/W
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	110	°C/W

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 5)						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250uA	BV_{DSS}	600	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250uA	$V_{GS(TH)}$	2.5	3.6	4.5	V
Gate Body Leakage	V_{GS} = ±30V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = 600V, V_{GS} = 0V	I_{DSS}	--	--	10	uA
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 1A	$R_{DS(ON)}$	--	3.9	4.4	Ω
Forward Transfer Conductance	V_{DS} = 40V, I_D = 1A	g_{fs}	--	1.5	--	S
Dynamic (Note 6)						
Total Gate Charge	V_{DS} = 480V, I_D = 2A, V_{GS} = 10V	Q_g	--	9.4	--	nC
Gate-Source Charge		Q_{gs}	--	2.2	--	
Gate-Drain Charge		Q_{gd}	--	4.7	--	
Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	249	--	pF
Output Capacitance		C_{oss}	--	30.7	--	
Reverse Transfer Capacitance		C_{rss}	--	5	--	
Gate Resistance	F = 1MHz, open drain	R_g	--	8.5	--	Ω
Switching (Note 7)						
Turn-On Delay Time	V_{GS} = 10V, I_D = 2A, V_{DD} = 300V, R_G =25Ω	$t_{d(on)}$	--	9.1	--	ns
Turn-On Rise Time		t_r	--	9.8	--	
Turn-Off Delay Time		$t_{d(off)}$	--	17.4	--	
Turn-Off Fall Time		t_f	--	12.4	--	

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Source-Drain Diode (Note 5)						
Diode Forward Voltage	I_S = 2A, V_{GS} = 0V	V_{SD}	--	0.9	1.4	V
Reverse Recovery Time	V_{GS} = 0V, I_S =2A, dI_F/dt = 100A/us	t_{rr}	--	490	--	ns
Reverse Recovery Charge		Q_{rr}	--	0.8	--	µC
Source Current	Integral reverse diode in the MOSFET	I_S	--	--	2	A
Source Current (Pulse)		I_{SM}	--	--	8	A

Notes:

1. Current limited by package.
2. Pulse width limited by the maximum junction temperature.
3. L = 25mH, I_{AS} = 2A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C.
   100% Eas Test Condition: L = 25mH, I_{AS} = 1A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
4. I_{SD} ≤ 2A, di/dt ≤ 200A/µs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25ºC.
5. Pulse test: PW ≤ 300µs, duty cycle ≤ 2%.
6. For DESIGN AID ONLY, not subject to production testing.
7. Switching time is essentially independent of operating temperature.

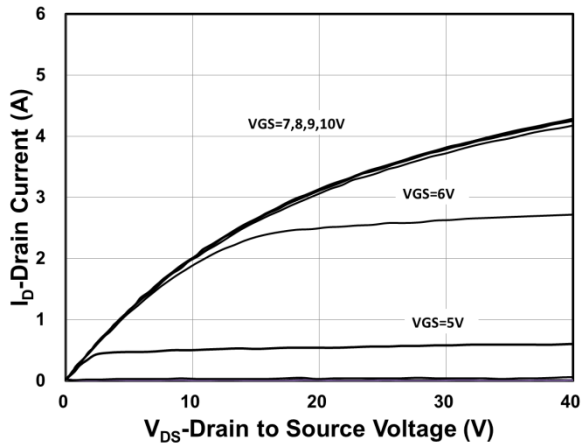
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM2NB60CH C5G	TO-251 (IPAK)	75pcs / Tube
TSM2NB60CP ROG	TO-252 (DPAK)	2,500pcs / 13” Reel

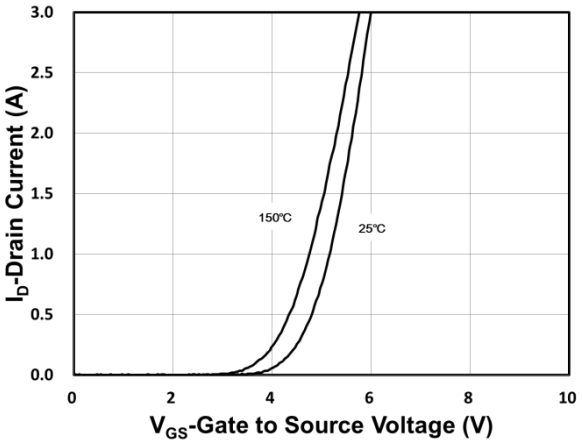
CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

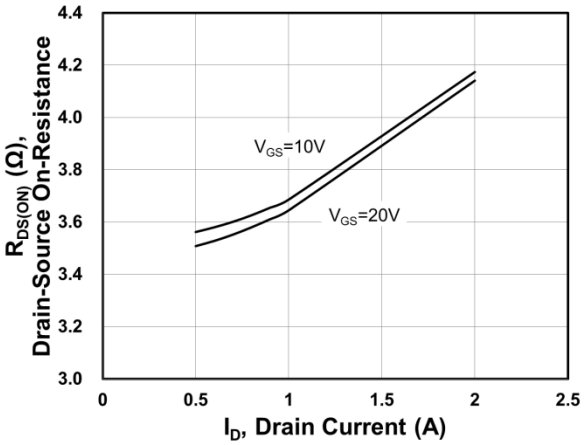
Output Characteristics



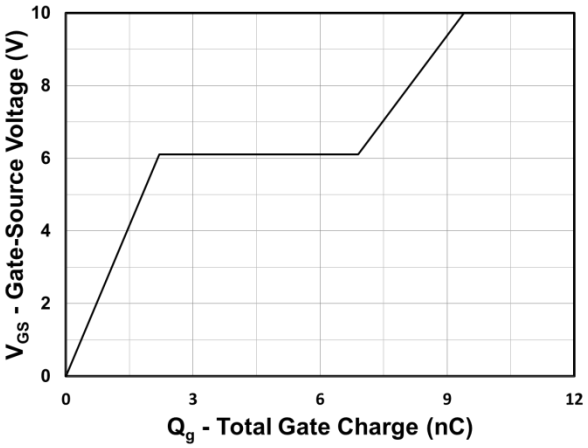
Transfer Characteristics



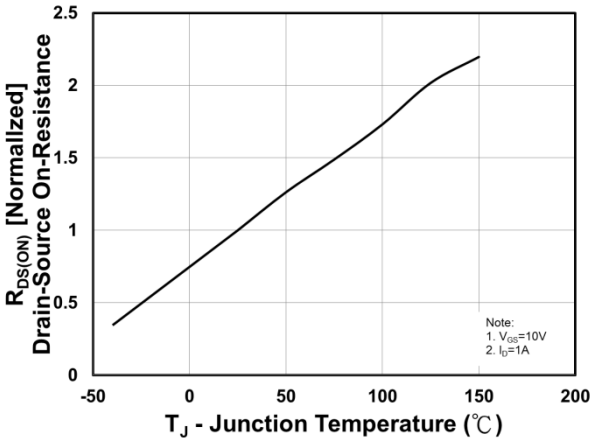
On-Resistance vs. Drain Current



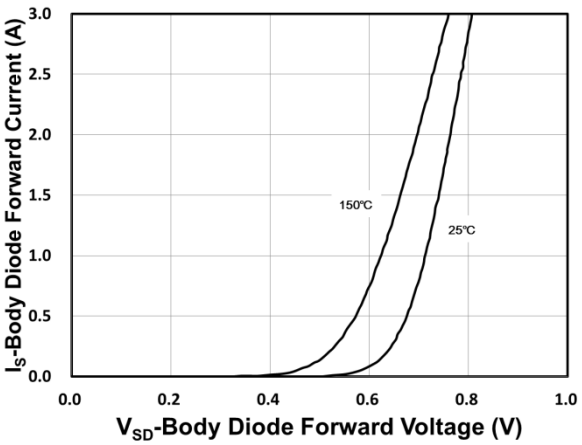
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



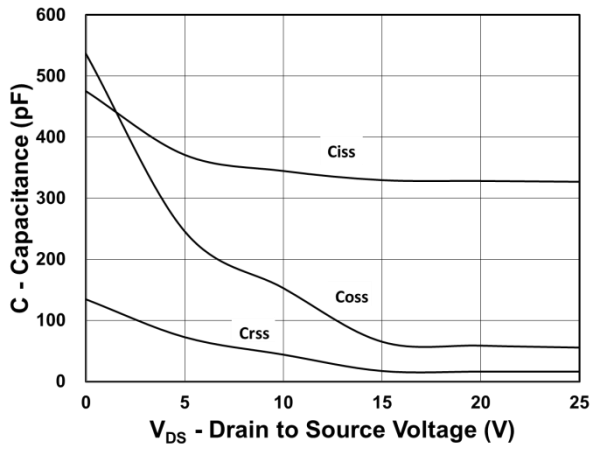
Source-Drain Diode Forward Current vs. Voltage



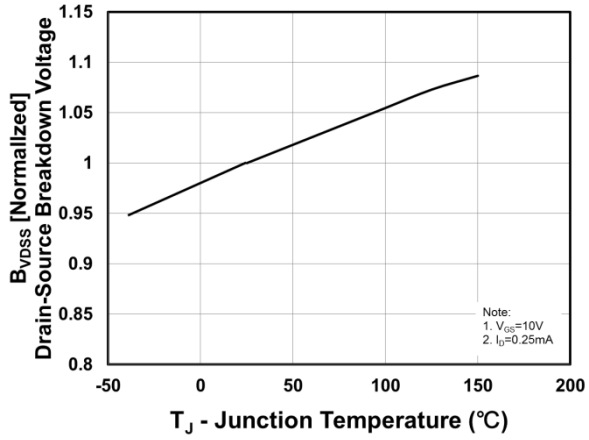
CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

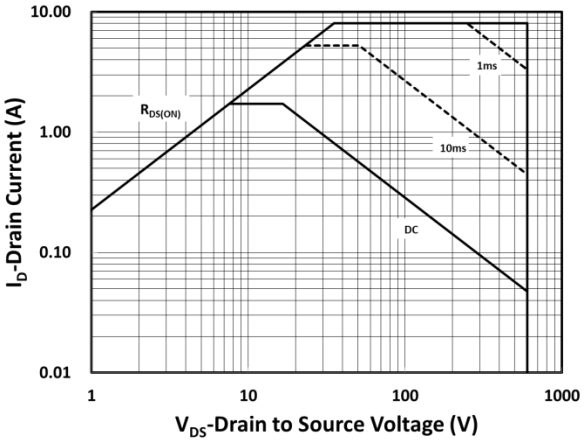
Capacitance vs. Drain-Source Voltage



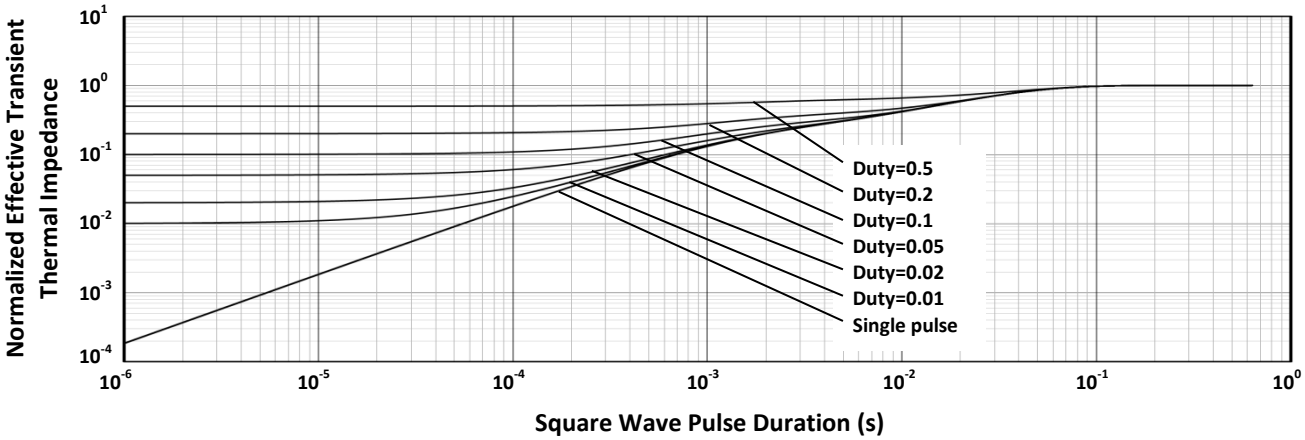
BV_{DSS} vs. Junction Temperature



Maximum Safe Operating Area

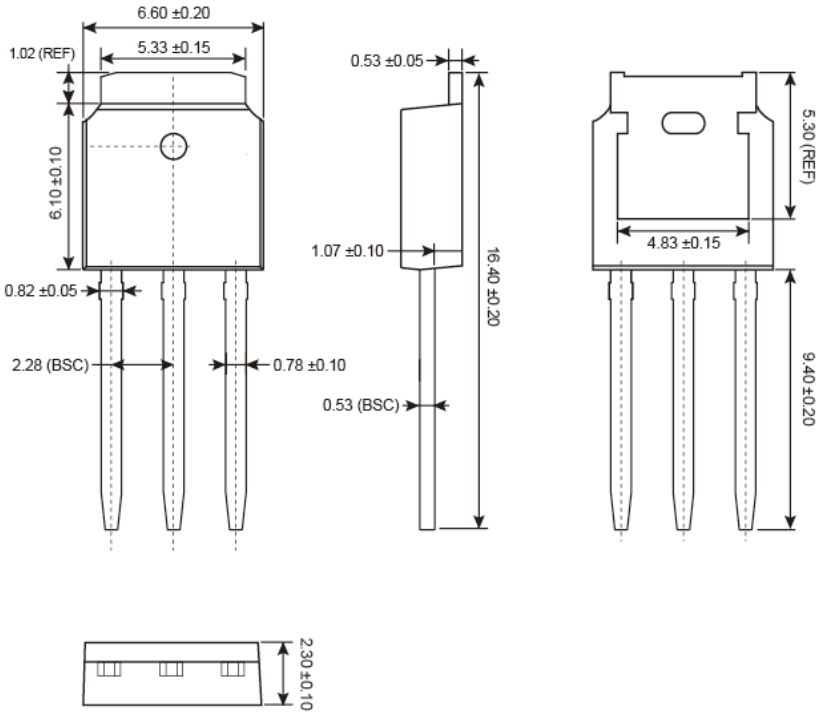


Normalized Thermal Transient Impedance, Junction-to-Case

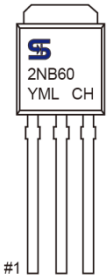


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-251(IPAK)



MARKING DIAGRAM



Y = Year Code

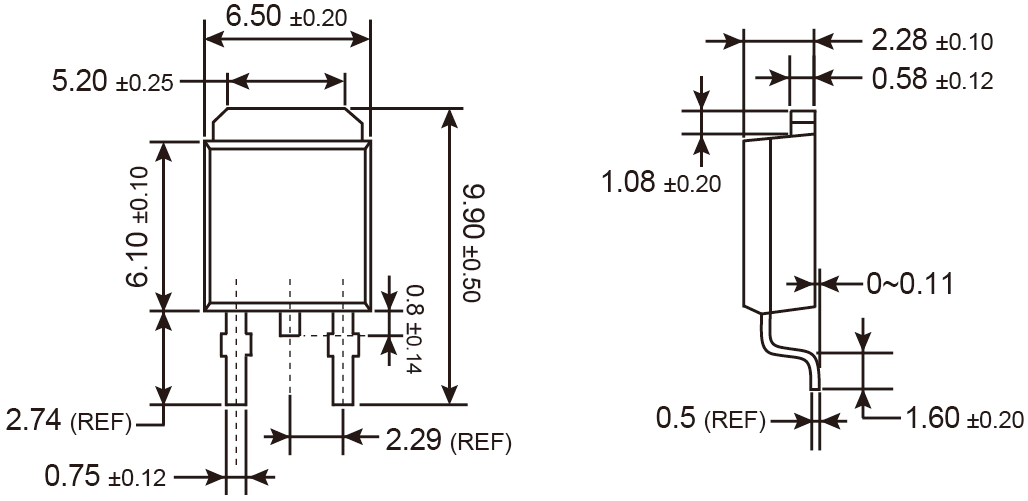
M = Month Code for Halogen Free Product

O	=Jan	**P**	=Feb	**Q**	=Mar	**R**	=Apr
S	=May	**T**	=Jun	**U**	=Jul	**V**	=Aug
W	=Sep	**X**	=Oct	**Y**	=Nov	**Z**	=Dec

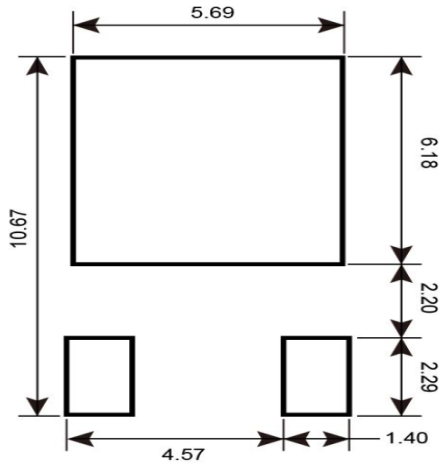
L = Lot Code (1~9, A~Z)

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

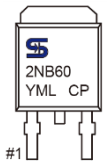
TO-252(DPAK)



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



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